Jae-Won Jang

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EDUCATION

Virginia Tech — **Blacksburg, VA**
Ph.D. candidate in Computer Engineering, GPA: 3.74 / 4.00 — Expected May 2024

University of South Florida — **Tampa, FL**
MS, Computer Engineering, GPA: 3.76 / 4.00 — Jan 2014 – Aug 2015
Thesis Title: Security of Non-Volatile Memories – Attack Models, Analyses, and Counter-Measures
BS, Computer Engineering, GPA: 3.69 / 4.00 | Engineering GPA: 3.83 / 4.00 — Aug 2009 – Dec 2013

RESEARCH & TEACHING EXPERIENCE

Virginia Tech — **Blacksburg, VA**
Research Assistant — Aug 2018 - Present

- Primary research focus is system and software security.
- Currently researching how to automatically generate compartmentalization policy and apply compartmentalization(s) on data in a fine-grained manner. To achieve this, developing a transpiler (source-to-source compiler) that inputs a source code and generates a compartmentalized assembly code after applying various analyses and optimizations.
- Established the soundness of code-diversified binaries by verifying functional equivalence to its original binary. We proposed a methodology that inputs an assembly code and performs symbolic execution to check for stuttering bisimulation to prove that code-diversified and original binaries are semantically equivalent.
- Explored an alternative approach to enhance existing control-flow integrity (CFI) techniques by protecting the binary from the *adversary's* perspective. We proposed a technique that generates a forbidden list of addresses for an input binary and applies binary rewriting to harden the binary to perform a runtime check to deny malicious access.
- Developed a framework that inputs a source code first to apply static taint analysis to determine potentially sensitive data that adversaries can use to exploit. Afterward, the framework compartmentalizes the sensitive data of vulnerable programs by relocating the data to a random location and applying the latest hardware primitive such as ARM Memory Tagging Extension (MTE).

Penn State University — **State College, PA**
Teaching Assistant — Fall 2017

- Instructed the course (CMPSC 122 – Intermediate Programming - Python data structure course) for undergraduate students.

Research Assistant — Fall 2016 – Summer 2017

- Research focused on hardware security involving reverse engineering and gate camouflaging techniques.
- Researched a way to camouflage interconnect between multiple gates by modulating the threshold voltage of transistors.
- Proposed a design of a multi-input camouflaged gate that can perform six complex Boolean functions.

University of South Florida — **Tampa, FL**
Graduate-level Tutor — Spring 2014 - Spring 2015

- Tutored USF INTO pathway system students on graduate-level computer engineering courses: Operating Systems, Introduction to Theory of Algorithms, and Computer Architecture.

Research Assistant — Fall 2013 - Summer 2016

- Research focused on employing CMOS and emerging memory technology (spintronics) to develop security primitives.
- Designed layouts (utilized up to M8 layer) of non-volatile sequential elements and schematics using a 65nm library; Completed 1-tapeout of padframe.
- Investigated the property of Spin-transfer Torque (STT)-mRAM to analyze vulnerabilities against magnetic and thermal attacks.
- Proposed various ways to improve the stability of Physically Unclonable Function (PUF) and a novel way of utilizing Magnetic Tunnel Junction (MTJ) to improve the robustness of an SRAM while minimizing leakage and area overhead.

JOB EXPERIENCE

Raytheon — **State College, PA**
Software Engineer — Dec 2017 – July 2018

- Aided other Raytheon employees in non-security clearance tasks while waiting for the security clearance

Intel **Hillsboro, OR**

Undergraduate Intern Summer 2013

- Was tasked with utilizing Intel AIM Suite APIs on digital price tag prototype to gather information about the audience for products sold in the supermarket and constructing a user tutorial for the AIM Suite.
- Investigated a reason for the memory leak of the digital price tag prototype and proposed a temporary solution.

PUBLICATIONS (6 first-author publications and 6 co-authored publications)

JOURNALS (J):

1. **Jae-Won Jang**, Asmit De, Deepak Vontela, Ithihasa Nirmala, Swaroop Ghosh, and Anirudh Iyengar, "Threshold-defined Logic and Interconnect for Protection against Reverse Engineering", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**) (Impact Factor: 2.09)
2. Anirudh Iyengar, Swaroop Ghosh, and **Jae-Won Jang**, "MTJ-based State Retentive Flip-Flop with Enhanced-Scan Capability to Sustain Sudden Power Failure", Transactions on Circuits and Systems I (**TCAS-I**). (Impact Factor: 2.3)
3. Swaroop Ghosh, Anirudh Iyengar, Seyedhamidreza Motaman, Rekha Govindaraj, **Jae-Won Jang**, Jinil Chung, Jongsun Park, Xin Li, Rajiv Joshi, and Dinesh Somasekhar, "Overview of Circuits, Systems, and Applications of Spintronics", IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS). (Impact Factor: 1.6)
4. Anirudh Iyengar, Kenneth Ramclam, Swaroop Ghosh, **Jae-Won Jang** and Cheng-Wei Lin, "Spintronic PUFs for Security, Trust and Authentication", ACM Journal of Emerging Topics Computing Systems (**JETC Special Issue**). (Impact Factor 0.83)

CONFERENCES (C):

1. **Jae-Won Jang,** Freek Verbeek, and Binoy Ravindran, "Verification of Functional Correctness of Code Diversification Techniques." NASA Formal Methods Symposium (**NFM**). Springer, Cham, 2021
2. Anirudh Iyengar, Deepak Vontela, Ithihasa Reddy, Swaroop Ghosh, Syedhamidreza Motaman, and **Jae-Won Jang "**Threshold Defined Camouflaged Gates in 65nm Technology for Reverse Engineering Protection", Proceedings of the International Symposium on Low Power Electronics and Design (**ISLPED**), 2018
3. Alexander Holst, **Jae-Won Jang** and Swaroop Ghosh, "Investigation of Magnetic Field-Based Attacks on Magnetoresistive Random-Access Memory", International Symposium on Quality Electronic Design Conference (**ISQED**), 2017
4. **Jae-Won Jang** and Swaroop Ghosh, "Performance Impact of Magnetic and Thermal Attack on STTRAM and Low-Overhead Mitigation Techniques", The International Symposium on Low Power Electronics and Design (**ISLPED**), 2016.
5. Swaroop Ghosh, Nasim Khan, Asmit De, **Jae-Won Jang**, "Security and Privacy Threats to On-Chip Non-Volatile Memories and Countermeasures", Proceedings of the 35th International Conference on Computer-Aided Design (**ICCAD '16**), 2016
6. **Jae-Won Jang,** Asmit De and Swaroop Ghosh, "Recent Trends in Intellectual Property (IP) Protection from Reverse Engineering", Microprocessor Test and Verification Conference (MTV), 2016 (Invited Paper)
7. **Jae-Won Jang**, Jongsun Park, Swaroop Ghosh, and Swarup Bhunia, "Self-Correcting STTRAM under Magnetic Field Attacks", Design Automation Conference (**DAC**), 2015
8. **Jae-Won Jang** and Swaroop Ghosh, "Design and Analysis of Novel SRAM PUFs with Embedded Latch for Robustness", International Symposium on Quality Electronic Design Conference (**ISQED**), 2015

ARCHIVES (arXiv) & WORK-IN-PROGRESS & DEMONSTRATIONS & INVENTION DISCLOSURES

1. Anirudh Iyengar, Kenneth Ramclam, **Jae-Won Jang** & Cheng Wei Lin, Spintronic PUFs for Security, Trust and Authentication, Cyber Security Awareness Week Conference (CSAW), 2014. (3rd Place / **Demonstration**)
1. Syedhamidreza Motaman, Swaroop Ghosh, **Jae-Won Jang,** Anirudh Iyengar, Rekha Govindaraj, Zakir Khondker, **"**A Reference-less Slope Detection Technique in 65nm for Robust Sensing of 1T1R Arrays", **arXiv,** 2023
2. Alexander Holst, Swaroop Ghosh, and **Jae-Won Jang,** "Investigation of Magnetic Field-Based Attacks on Magnetoresistive Random-Access Memory (**Work-in-Progress)**,**"** IEEE International Symposium on Hardware Oriented Security and Trust (**HOST**), 2016.
3. Volatile Flip-Flop with Enhanced-Scan Capability to Sustain Sudden Power Failure, Swaroop Ghosh, Anirudh Iyengar, and **Jae-Won Jang,** United States patent US 9,728,241.2017 Aug 8. (**Invention Disclosures)**

SKILLS & RESEARCH INTERESTS

Skills: Proficient in programming with C, Assembly Language, and Python; Familiar with TensorFlow, OpenCV, C++, Java, Haskell

Research Interests: Systems Engineering, Systems/Software Security, Computer Architecture, Compilers, Verification

Languages: Korean (native), English (native), Japanese (Beginner)

Interests: Tennis, running, weightlifting, cooking, board games, hiking, group activities